MF520
3-Phase Brushless DC Motor Controller
Data Sheet

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Table of Contents

Revision History:

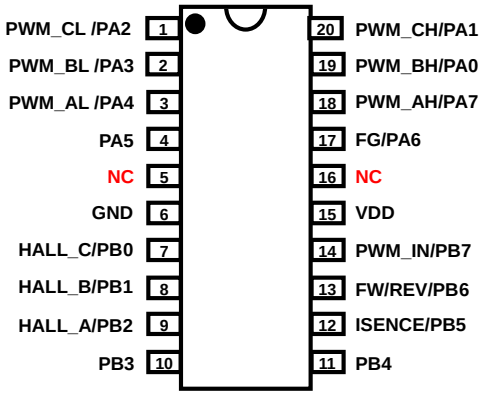
Revision	Date	Description
0.00	2020/01/07	Preliminary version
0.01	2020/04/14	1. Amend Chapter 1 and Section 3.1: Operating Temperature 2. Update DC/AC Characteristics: V_{DD}, f_{SYS}, R_{PH}, f_{IHRC}, f_{ILRC}, ADos
0.02	2020/12/09	1. Amend Supply Voltage/ Operating Voltage 2. Amend Input Voltage
0.03	2021/01/15	Add pin description
0.04	2022/12/12	Amend pin description

1. Key Features

- 3-Phase brushless DC motor with hall IC interface
- Sine wave / square wave
- PWM or voltage control input
- FG output
- Software hall degree forward
- Close loop or/and open loop control
- Current limit and over-current protection
- Lock-protect and auto-restart
- System protection
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
- MTP Programming
  - Support 6-wire factory programming mode
  - Support 4-wire in-system programming mode
- BLDC Applications
  - Operating voltage range: 3.5V~6V
  - Operating temperature range: -40°C~85°C
- Ordering/ Package Information
  - MF520-Y20: SSOP20 (150mil)

MF520 is a 3-phase BLDC motor controller based on 8-bit 8-FPPA MCU which can be programmed by 6-wire factory mode or 4-wire ISP mode. MF520 receives motor position signal from Hall IC and can control the sine wave or six step square wave flexibly to make the best efficiency of the motor. Through the PADAUK patented AP development system, it can easily set any speed curve, output signal and protection parameters etc., and it can observe the motor response online immediately. Using the MF520's development system, it's much easier and adjustable for application.

2. Pin Diagram and Pin Description



MF520 (SSOP20-150mil)

Pin Name	I/O	Description
PWM_CL / PA2	Output	C output signal to control the low side of motor driver
PWM_BL / PA3	Output	B output signal to control the low side of motor driver
PWM_AL / PA4	Output	A output signal to control the low side of motor driver
PA5	I/O	Digital input / digital output / analog input
GND	-	Ground
HALL_C / PB0	Input	Digital input to sense motor position C
HALL_B / PB1	Input	Digital input to sense motor position B
HALL_A / PB2	Input	Digital input to sense motor position A
PB3	I/O	Digital input / digital output / analog input
PB4	I/O	Digital input / digital output / analog input
ISENSE / PB5	Input	Analog input to sense motor current
FW/REV / PB6	Input	Forward / Reverse control input
PWM_IN / PB7	Input	PWM control input
VDD	-	Positive power
FG / PA6	Output	Rotation speed detection
PWM_AH / PA7	Output	A output signal to control the high side of motor driver
PWM_BH / PA0	Output	B output signal to control the high side of motor driver
PWM_CH / PA1	Output	C output signal to control the high side of motor driver

3. Device Characteristics

3.1. Absolute Maximum Ratings

Name	Min	Typ.	Max	Unit	Notes
Supply Voltage (VDD)	3.5		6	V	**Exceed the maximum rating may cause permanent damaged !!**
Input Voltage	-0.3		V_{DD} + 0.2	V	
Operating Temperature	-40		85	°C	
Storage Temperature	-50		125	°C	
Junction Temperature		150		°C	

3.2. DC/AC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
V_{DD}	Operating Voltage	3.5	5.0	6	V	-40 °C <Ta<85 °C
V_{FSV}	Forbidden V_{DD} startup voltage range	0.7		1.6	V	
V_{PORV}	V_{DD} power down release voltage			0.7	V	
T_{POR}	V_{DD} power on time (V_{DD} from 0V to 5V)			50	ms	
T_{FSV}	V_{DD} power on time during V_{FSV} range			10	ms	
f_{SYS}	System clock IHRC IHRC Internal low RC oscillator	 0 0	 33.8K	 8M 4M	 Hz	 V_{DD} = 3.3V V_{DD} = 2.5V V_{DD} = 5.0V
I_{OP}	Operating Current		1.8 3.5 150 8		mA mA uA uA	f_{SYS}=1MIPS@5.0V f_{SYS}=8MIPS@5.0V f_{SYS}=ILRC ~ 32KHz@5.0V f_{SYS}=ILRC ~ 12KHz@3.3V
I_{PD}	Power Down Current (by ***stopsys*** command)		3 1		uA uA	V_{DD}=5.0V V_{DD}=3.3V
I_{PS}	Power Save Current (by ***stopexe*** command)		0.4		mA	VDD=5.0V; Band-gap, LVD, IHRC, ILRC, Timer16 modules are ON.
V_{IL}	Input low voltage for IO lines	0		0.2V_{DD}	V	
V_{IH}	Input high voltage for IO lines	0.8 V_{DD}		V_{DD}	V	
I_{OL}	IO lines sink current	11	14	17	mA	V_{DD}=5.0V, V_{OL}=0.5V
I_{OH}	IO lines drive current	-8	-10	-12	mA	V_{DD}=5.0V, V_{OH}=4.5V
R_{PH}	Pull-high Resistance		90 170		KΩ	V_{DD}=5.0V V_{DD}=3.3V

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
V_{BRD}	Low Voltage Detect Voltage * (Brown-out voltage)	4.2 3.7 3.35 3.25 3.05 2.9 2.75 2.47	4.5 4 3.75 3.5 3.3 3.15 3 2.7	4.8 4.3 4.05 3.75 3.55 3.4 3.25 2.93	V	
V_{BG}	Band-gap Reference Voltage (before calibration)	1.12	1.20	1.28	V	V_{DD}=5V, 25ºC
	Band-gap Reference Voltage * (after calibration)	1.17*	1.20*	1.23*		V_{DD}=2.5V ~ 5.5V, -40ºC <Ta<85ºC*
f_{IHRC}	Frequency of IHRC after calibration *	15.52*	16*	16.48*1 6.32*	MHz	25ºC, V_{DD}=3V~5.5V
		15*	16*	17.28*		V_{DD}=3V~5.5V, -40ºC <Ta<105ºC*
f_{ILRC}	Frequency of ILRC *	20.4*	24*	27.6*	KHz	V_{DD}=5.0V, Ta=25ºC
		15.6*	24*	32.4*		V_{DD}=5.0V, -40ºC <Ta<85ºC*
		10.2*	12*	13.8*		V_{DD}=3.3V, Ta=25ºC
		7.8*	12*	16.2*		V_{DD}=3.3V, -40ºC <Ta<85ºC*
V_{ADC}	Workable ADC operating Voltage	2.5		5.0	V	
V_{AD}	AD Input Voltage	0		V_{DD}	V	
ADrs	ADC resolution			11	bit	
ADclk	ADC clock period		2		us	2.5V ~ 5.5V
t_{ADCONV}	ADC conversion time (T_{ADCLK} is the period of the selected AD conversion clock)		14		T_{ADCLK}	
AD DNL	ADC Differential NonLinearity		±3*		LSB	
AD INL	ADC Integral NonLinearity		±3*		LSB	
ADos	ADC offset*		3 4		LSB	-40ºC <Ta<85ºC* -40ºC <Ta<105ºC*
t_{INT}	Interrupt pulse width	30			ns	V_{DD} = 5.0V
V_{DR}	RAM data retention voltage*	1.5			V	In power-down mode.
t_{WDT}	Watchdog timeout period (T_{ILRC} is the clock period of ILRC)		4096			misc[1:0]=01
			16384			misc[1:0]=10
t_{SBP}	System boot-up period from power-on		1024		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
t_{WUP}	System wake-up period					
	Fast wake-up by IO toggle from STOPEXE suspend		128		T_{SYS}	Where T_{SYS} is the time period of system clock
	Fast wake-up by IO toggle from STOPSYS suspend, IHRC is the system clock		128 T_{SYS} + T_{SIHRC}			Where T_{SIHRC} is the stable time of IHRC from power-on.
	Fast wake-up by IO toggle from STOPSYS suspend, ILRC is the system clock		128 T_{SYS} + T_{SILRC}			Where T_{SILRC} is the stable time of ILRC from power-on.
	Normal wake-up from STOPEXE or STOPSYS suspend		1024		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC
HCPos	Comparator offset*	-	±10	±20	mV	
HCPcm	Comparator input common mode*	0		V_{DD}-1.5	V	
HCPspt	Comparator response time**		100	500	ns	Both Rising and Falling
HCPmc	Stable time to change comparator mode		2.5	7.5	us	

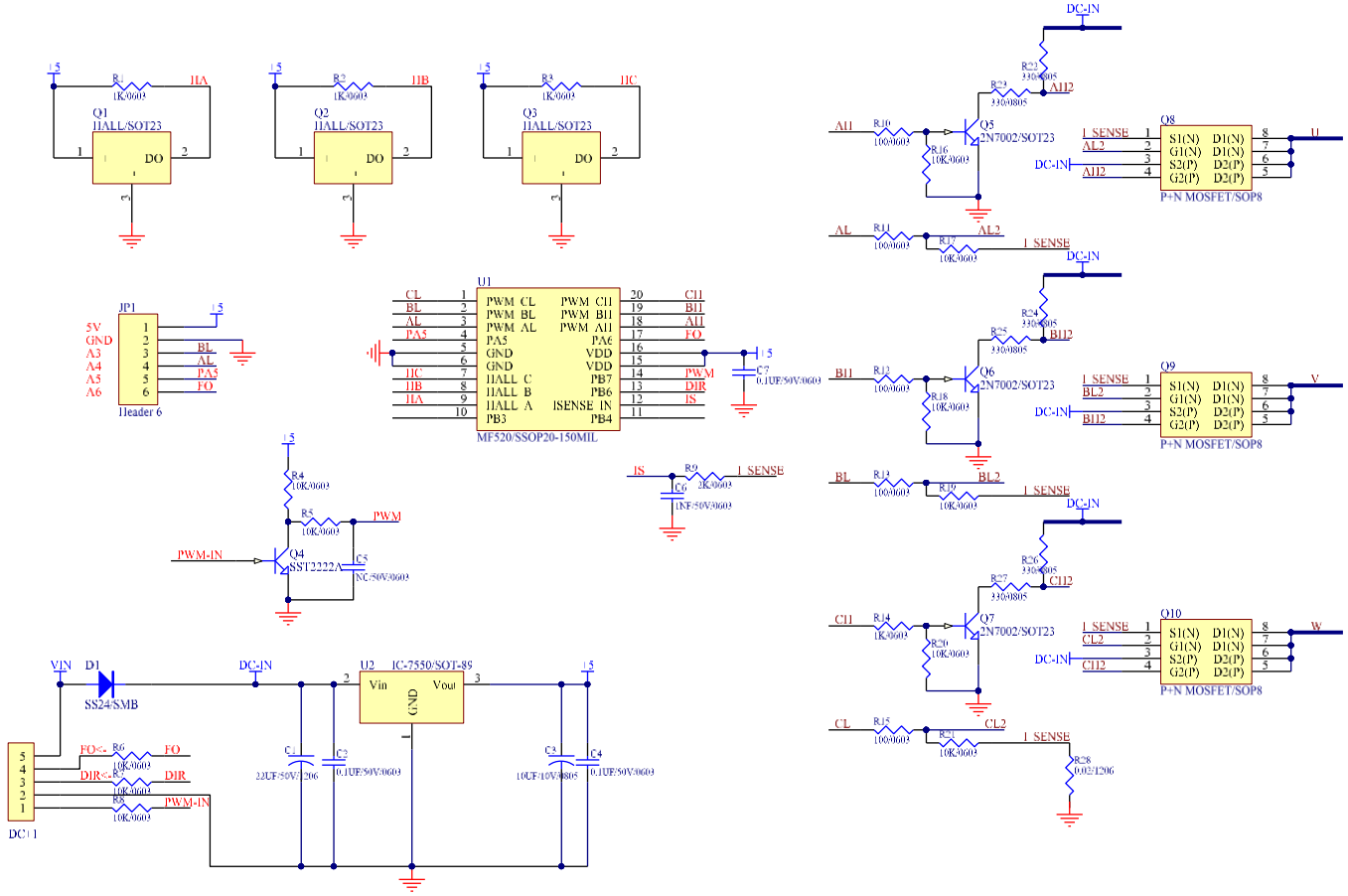
*These parameters are for design reference, not tested for every chip.

** Response time is measured with comparator input at (V_{DD}-1.5)/2 -100mV, and (V_{DD}-1.5)/2+100mV

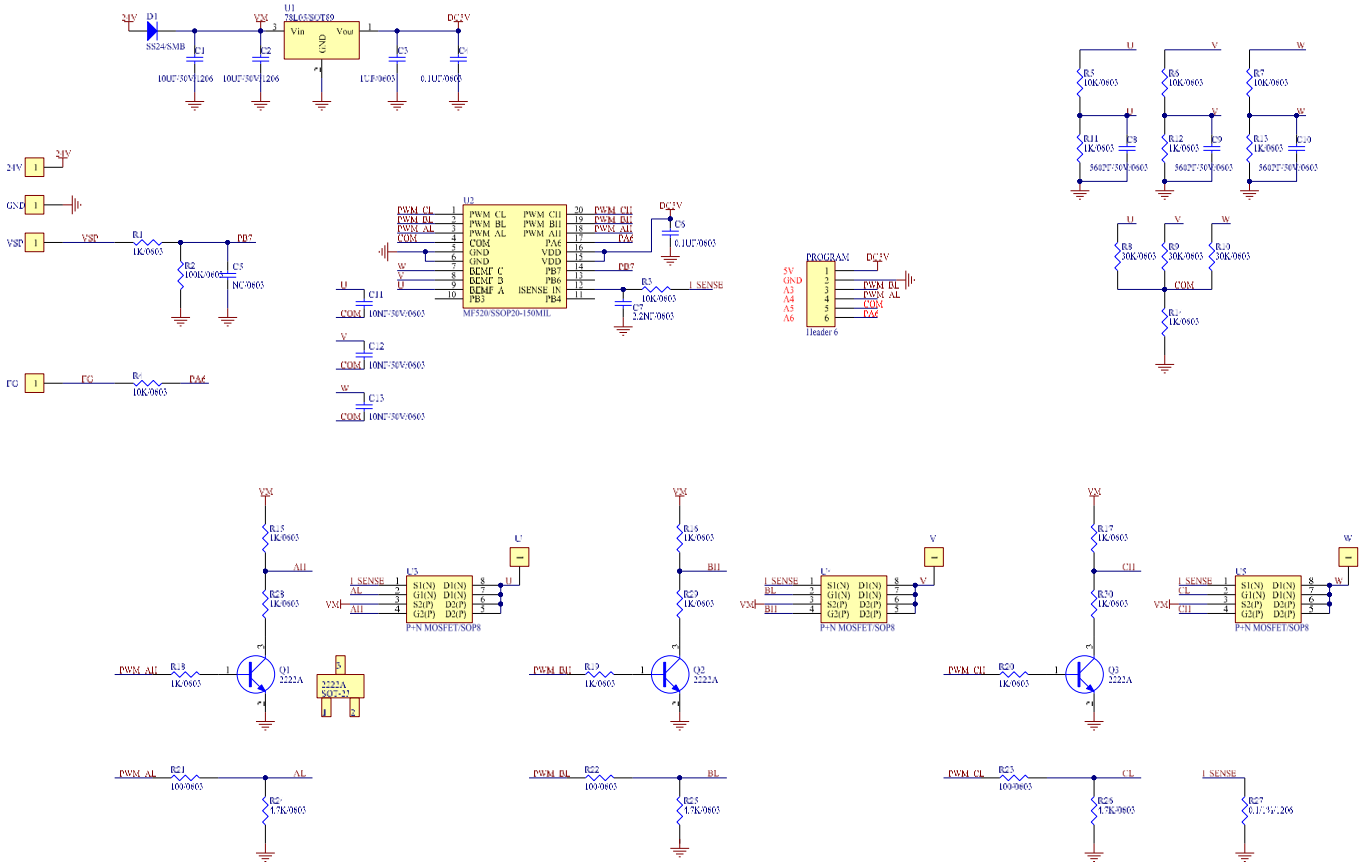
The characteristic diagrams are the actual measured values. Considering the influence of production drift and other factors, the data in the table are within the safety range of the actual measured values.

4. Reference Application Circuit

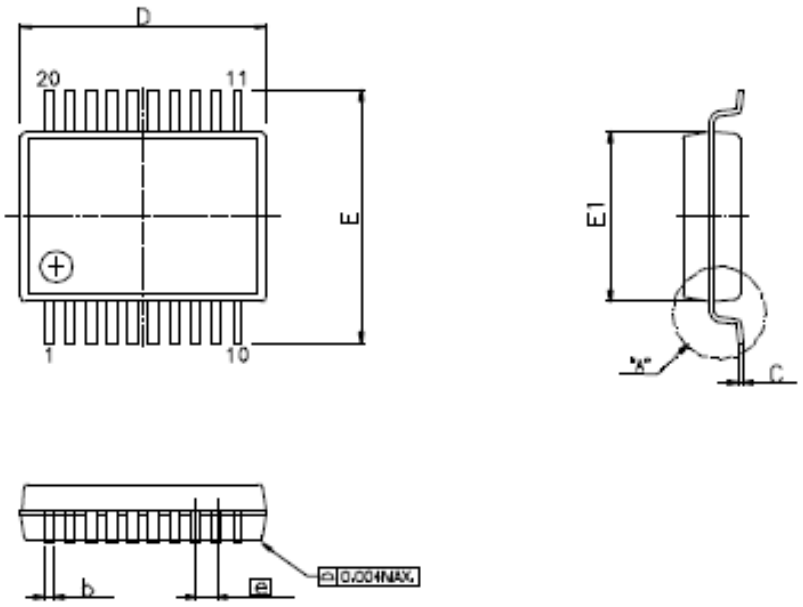
4.1. 3HALL



4.2. Sensor-less



5. Package Information: SSOP20 (150mil)



DETAIL : A

	INCH		
SYMBOLS	MIN	TYP	MAX
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	-	-	0.059
b	0.008	-	0.012
C	0.007	-	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e		0.025 BSC	
L	0.016	0.025	0.050
L1		0.041 BSC	
θ °	0	-	8