6S-M-001

User Manual

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Revision History:

Revision	Date	Description
0.00	2021/05/18	1st Version
0.01	2021/11/10	1. Update the name of 6S-M-001 2. Update image in section 2.1&2.4
0.02	2022/02/24	1. Add chips which 6S-M-001 supports to simulate 2. Add the description of multi-core operation mode 3. Update the description in Section 1.1

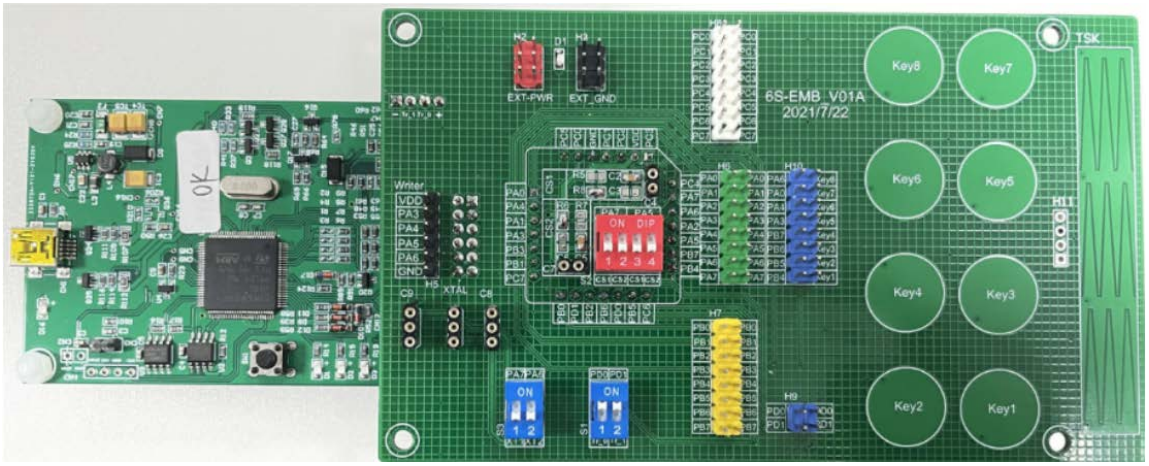
1. Foreword

PADAUK Technology provides the simulation tools 6S-M-001 emulator for touch IC. 6S-M-001 emulator should be combined with IDE software which is also developed by PADAUK Technology for normal simulation (Touch program can be generated by P-Touch).

6S-M-001 = 5S-P-C01 (Left) + 6S-EMB (Right) + 6S-EVB (Back of 6S-EMB)

EMB: Evaluation Main Board

EVB: Evaluation Board



This paper only introduces the usage of 6S-EMB and 6s-EVB in 6S-M-001.

About how to use 5S-P-C01, FPPA IDE and P-Touch, please refer to their user manuals：

http://www.padauk.com.tw/cn/technical/index.aspx?kind=36

1.1. Support IC series

Touch Series:

Support all series simulation (Except PMS160);

Other MCU Series:

Support multi-core simulation of PFC232;

Support simulation of PMS152/PFS172/PFS123 (with 11 bit PWM).

2. Recognize with 6S-EMB and 6S-EVB

2.1 Appearance of 6S-EMB

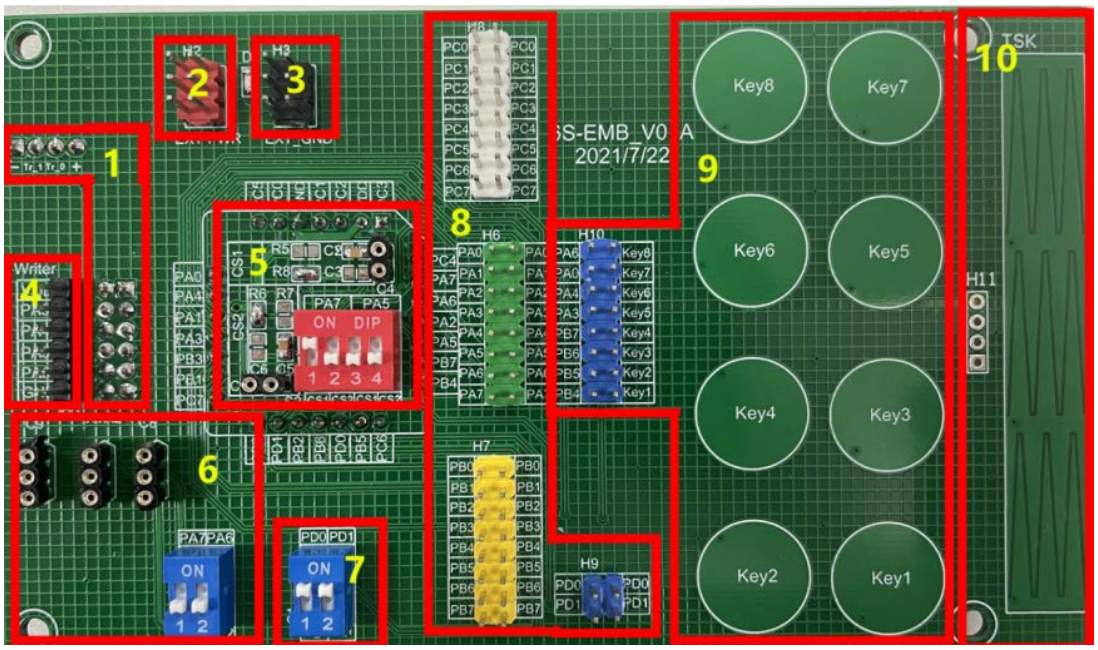


Fig. 1: Front of 6S-EMB

Fig. 2: Back of 6S-EMB

1. ICE Interface(H1, H4):

Connect with IO interface of 5S-P-C01.

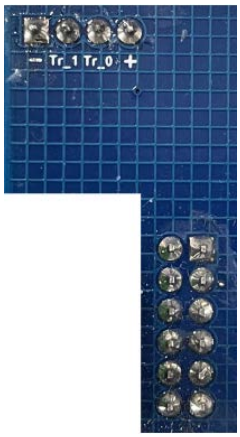


Fig. 3: Interface of H1 and H4

2. ICE Power output Interface(H2):

H2 is a common connection pin of 6Pin, which is powered by 5S-P-C01 (0V) with a positive power(+V) output interface. The text is marked as EXT-PWR.

Fig. 4: H2 Interface

3. ICE Power ground output Interface(H3):

H3 is a common connection pin of 6Pin, which is powered by 5S-P-C01 (0V) output interface (external common ground interface).The text is marked as EXT_GND.

Fig. 5: H3 Interface

4. Program Channel(H5):

Because of 6S-EMB connecting with 5S-P-C01, users can use the emulator to write directly. And writing method is the same to 5S-P-C01 (Please refer to 5S-P-C01 user manual for details).

Note that PD0 and PD1 at S1 (as shown in Figure 9) need to be turned off when using this emulation board to write.

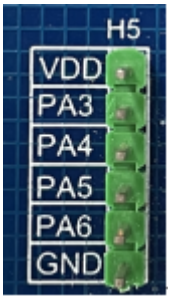


Fig. 6: H5 Interface

5. CS Selection Section:

DIP switch 1, 2 correspond to PA7 as CS PINS; DIP switch 3, 4 correspond to PA5 as CS PINS. DIP switch 1, 3 (CS1) is small capacitor (about 22nF); DIP switch 2, 4 (CS2) is bulk capacitor (about 33nF). Users can select to enable or disable the CS capacitor of the corresponding pin as required. However, PA7 and PA5 pins can not use CS at the same time. Also, CS cannot be enabled for the PA5 and PA7 pins at the same time. Users can also replace the CS capacitors on touch pad as required, but it is not recommended to replace it in case of unnecessary influence on the touch sensitivity. If users have any requirements, please contact with FAE at first for consulting.

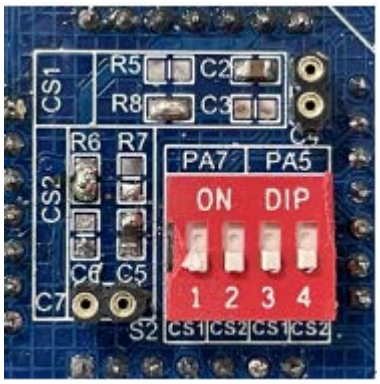


Fig. 7: CS Selection Section

6. Crystal Selection Section:

DIP switch 1, 2 on S3 are external crystal enable switch. To connect an external crystal oscillator, turn on both dip switches and connect the crystal oscillator to the XTAL port. C8 and C9 are crystal vibrating capacitor interfaces. Users need to match the vibrating capacitor of the crystal oscillator according to its specification.

Fig. 8: Crystal Selection Section

7. Communication Enable Section：

It is communication switch between 5S-P-C01 and 6S-EMB. DIP switch 1, 2 should be turned on when simulating, and must be turned off when writing.

Fig. 9: Communication Enable Section

8. IO Interface：

H6(PA0~PA7),H7(PB0~PB7),H8(PC0~PC7) and H9(PD0~PD1) are I/O interface of the emulator, which can be maximum compatible with 26 I/O and 24 touch channels of PFC460. To simulate touch function, use Dupont wire to connect pins which needed at H6-H9 to common connection pin on the right of H10, as shown in Fig.11.

Note: Dupont wire should not be too long, otherwise it will affect the touch sensitivity.

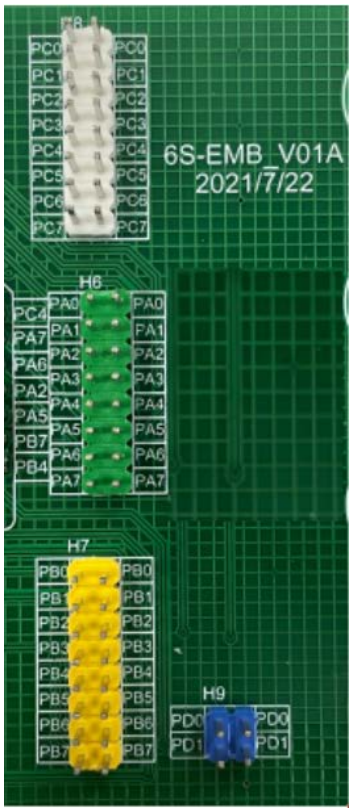


Fig. 10: IO Interface

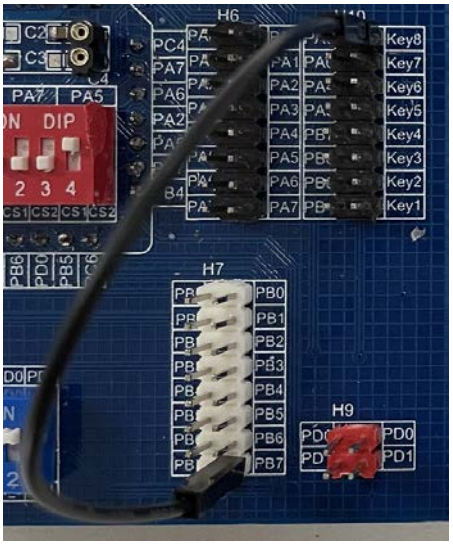


Fig. 11: PB7 Connects Key8 to enable touch

9. Touch PAD Section:

Common connection pin on the H10 right corresponds to Touch PAD Key1-Key8 in sequence. And Common connection pin on the left corresponds to PFC460 Channels TK1-TK8 in sequence. If users need to simulate other series IC or use the touch function of other IO, connect Dupont wire to common connection pin on the right side of H10.

Note: Dupont wire should not be too long, otherwise it will affect the touch sensitivity.

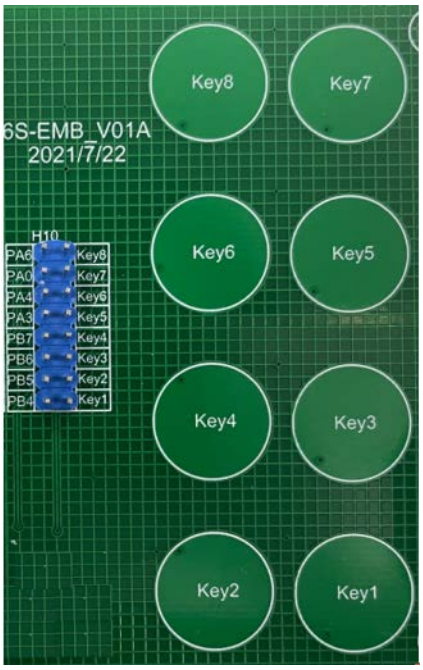


Fig. 12: Touch Pad Section

10. Slider Interface And Touch Control Slider Section

H11 is corresponding to 1-4 of the right slider from top to bottom, and the pins need to be welded by the user. Users can connect dupont wire to H11 from the touch channel chosen by H6-H9 as required, and at least two slide channels are needed. Please refer to Figure 11 for usage.

Fig. 13: Touch Control Slider Section

2.2 Description of 6S-EVB Appearance

U1 is simulation chip, which can simulate for 1000 times. If it can not simulate due to over the number of times, please contact with original factory for replacement.

Fig. 14: Front of 6S-EVB

Fig. 15: Back of 6S-EVB

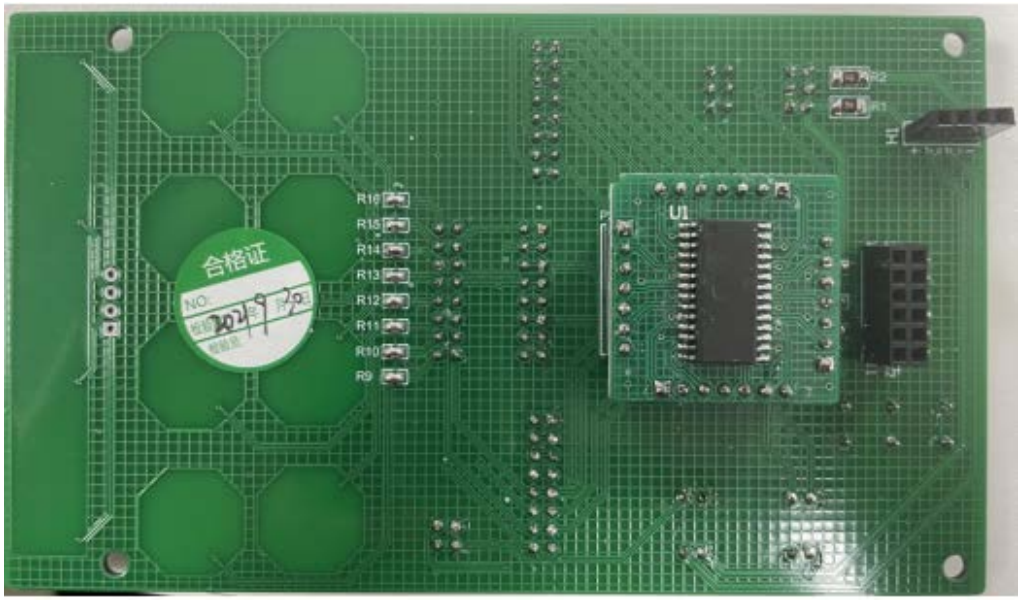


Fig. 16: Connection Diagram of 6S-EVB and 6S-EMB

2.3 Connection of 6S-EMB and 5S-P-C01

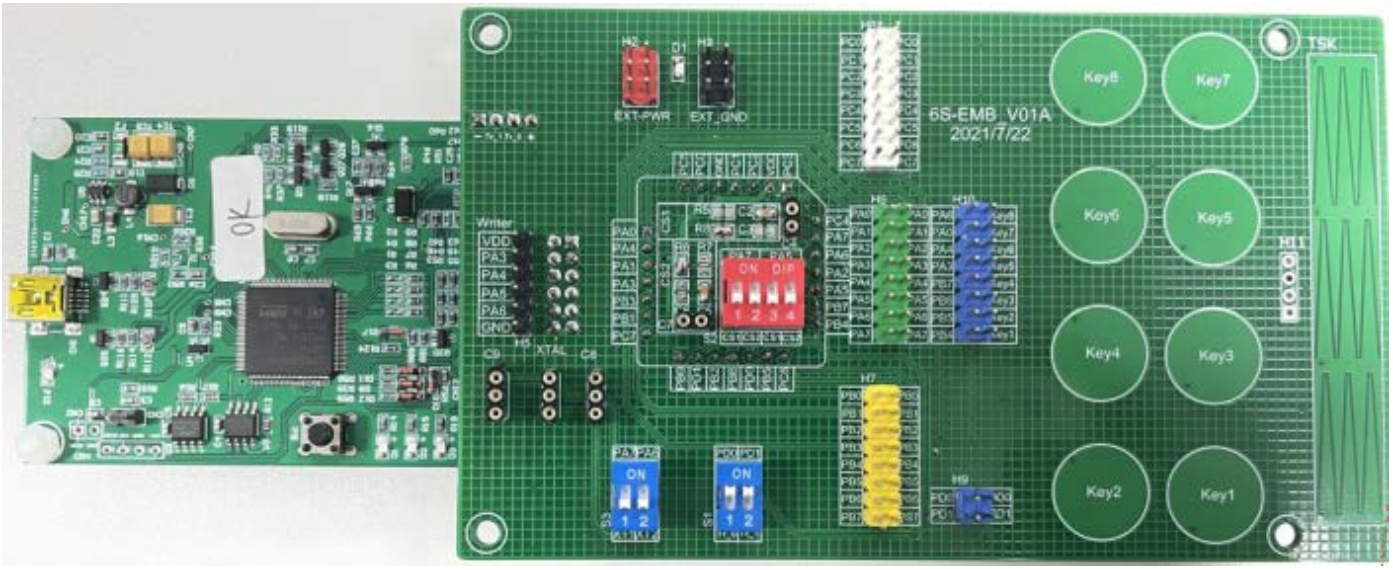


Fig. 17: Front of connection between 6S-EMB and 5S-P-C01

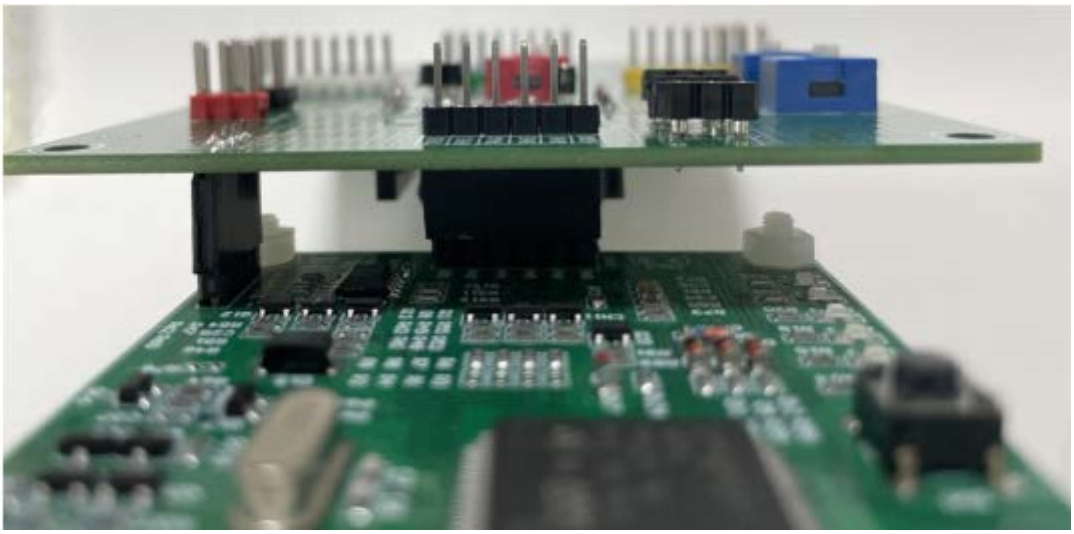


Fig. 18: Side of connection between 6S-EMB and 5S-P-C01

2.4 6S-EMB Schematic Diagram

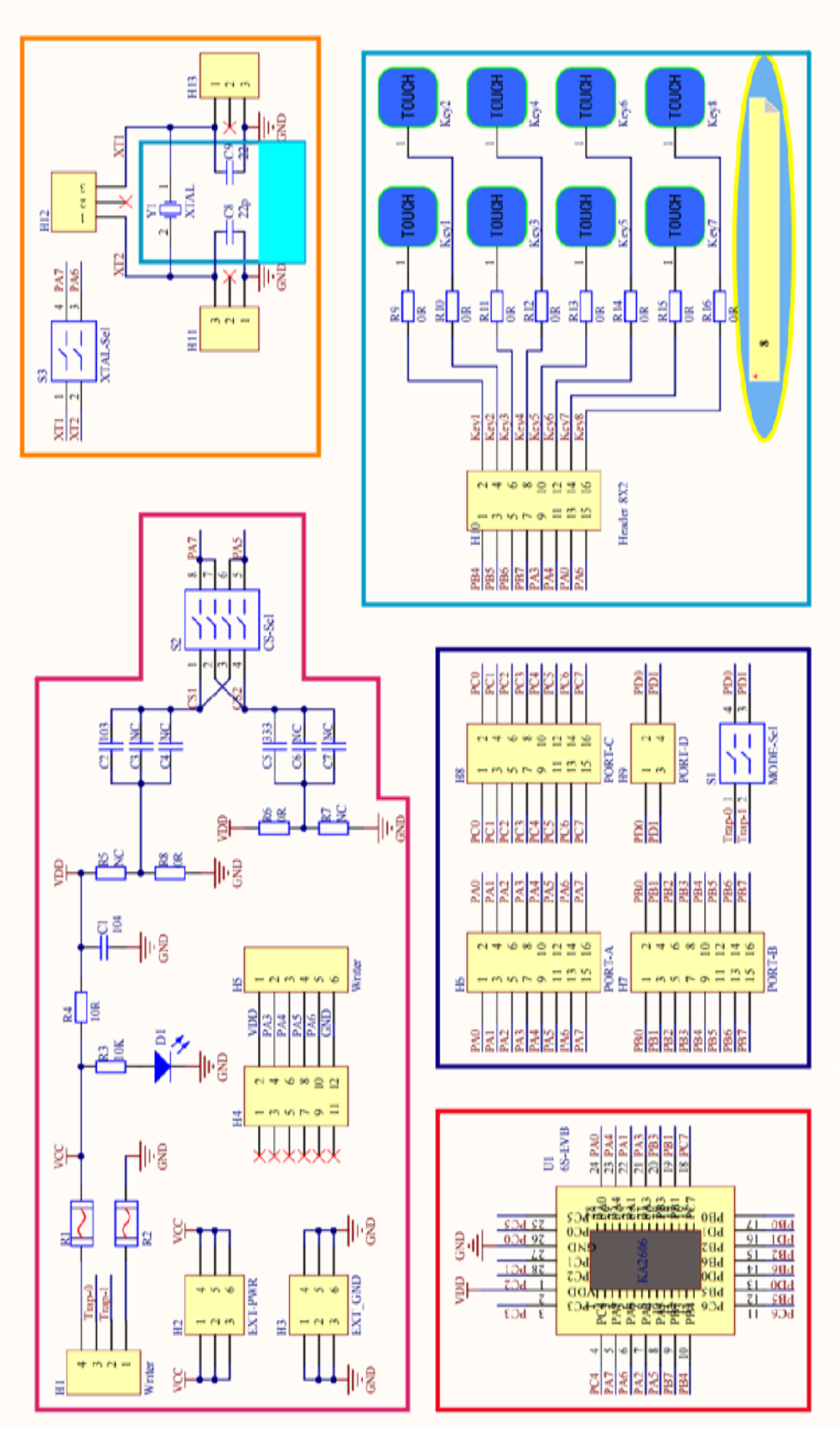


Fig. 19: 6S-EMB schematic diagram

3. 6S-M-001 Working Mode

6S-M-001emulator owns two work modes: The single-core (1 FPPA) simulation debugging mode and Single/multi-core operation mode at full speed

3.1 Single-core simulation debugging mode:

1. Only support single-core programme (FPPA0) to simulate debugging operation.
2. To use this mode, DIP-SW S1 on the emulator must be turned on.
3. To operate in this mode, the command “Writer Set_ISP_ICE” which is in ".PRE” file must be shielded.
4. When single-core simulation operate, system will occupy part of IC resource, so that the maximum available space and resource will be reduced.

   Maximum ROM Space: 0x000 ~ 0xD00 (3328 Words)；

   Maximum RAM Space: 0x000 ~ 0x1F7 (503 Bytes).
5. PD.0/PD.1 pins will be used by system as simulating communication interface. In this mode, operation to PD.0/PD.1 in programme will invalid. And the command for operating PDIER/PDC/PD register will be changed to NOP.
6. Related functions of PD.0/PD.1pins, please verify on the actual chip or by single/multi-core operation mode at full speed.

3.2 Single/multi-core operating mode at full speed:

1. Support single/multi-core programme operating at full speed.

2. In this mode, the “.Writer Set_ISP_ICE” command must be insert into “.PRE” file.

3. When the emulator operates at full speed, simulation chip resource will not be occupied by system, which is the same as actual chip.

4. In this mode, some common ICE operations are not supported, such as break point, pause and so on.

5. This mode supports simulating all common functions of PD.0 / PD.1 pin. After Load Coad, DIP-SW S1 on emulator must be turned off.

Note：Only PFC460 and PFC232 supply for multi-core simulating mode.

4. Notes for using 6S-M-001

1. To do the simulation function of Touch Key, 6S-EMB and 6S-EVB must be matched with 5S-P-C01.
2. 6S-M-001 can also simulate other function except touching.
3. Since Version 0.91C5, IDE starts to support 6S-M-001 simulation.
4. Since Version V1.6, P-Touch starts to support 6S-M-001 simulation.
5. When adjust any touch parameter (e.g. TK Channel, CS...) on 6S-EMB, simulation mode needs to re-access.